EET340 Programmable Hardware Technology Syllabus

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Textbook
"Digital System Designs and Practices: Using Verilog HDL and FPGAs**",** Ming-Bo Lin, Wiley and Son.

Lecture: Tuesday: 2:00-3:30 PM and Thursday: 1:00-2:50 PM
Classroom: **TE211B**

Course Contents:
Programmable logic design, simulation, synthesis, verification, and implementation using a Hardware Description Language (HDL). Industry standard tools, and prototyping hardware. Mixed-level modeling including gate-level, dataflow and behavioral levels. HDL language constructs and design techniques. Logic timing and circuit delay modeling. Programming Language Interface (PLI). Advanced verification techniques.

Tentative Schedule

Week	Contents
1	Overview of Verilog language
2	Verilog language construct and structural style modeling
3	Behavior style modeling
4	Data flow style modeling
5	Tasks, functions, and UDPs
6	Hierarchical structural modeling
7	Advanced modeling techniques
8	Combinational logic modules
9	Sequential logic modules (1)
10	Sequential logic modules (2)
11	Design options of digital systems
12	Sequential circuit
13	System design methodology (1)
14	System design methodology (2)
15	Synthesis

Homework:
Homework will be periodically given with prescribed due dates. **Assignments must be handed in at the beginning of class time on the specified due date.** In the event a hardcopy cannot be turned in at that time, an e-mail containing your completed and finished assignment as a word document, jpeg, or pdf will suffice. It should be expected that late assignments will be penalized at a rate of at least 25% per day. A week after the due date the assignments will no longer be accepted.

Attendance: Attendance at every scheduled class session is highly encouraged. Students who are habitually absent will be at a disadvantage. Students are responsible for all materials presented in class.

Project Assignments

1. Every project must be demonstrated to be working either in the simulator or hardware kit.
2. A report must be written after the project has been demonstrated to be working and is due one week after the project demonstration.

Grading:

90% - 100% A
80% - 89% B
70% - 79% C
60% - 69% D
0% - 59% F