EE 106 Introduction to Electrical/Computer Engineering I
Fall Semester 2016

Instructor: Dr. Nannan He
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Office hours: MW 9am to noon, Tuesday and Thursday 11am to noon or by appointment

Textbook: "*Fundamentals of Logic Design (7th)*", Charles H. Roth. Jr. and Larry L. Kenney, Cengage Learning Engineering, 2014.

Course Description: This introductory course covers digital systems topics including binary numbers, logic gates, Boolean algebra, circuit simplification using Karnaugh maps, flip-flops, counters, shift registers and arithmetic circuits. Problem solving methods, study skills and professional development will be addressed throughout the course.

Lecture: Monday and Wednesday 8am - 8:50am, WH 0289
Lab: 01: Thursday 8am-10:50am, TN N292; 02: Wednesday 2pm-4:50pm, TN N292; 03 and 40: Friday 9am-11:50am, TN N292;

Course Outcomes
1. Convert between number systems (e.g., binary, decimal, hexadecimal and binary-coded decimal). *(Unit 1 in the textbook)*
2. Perform operations of addition and subtraction using signed and unsigned binary numbers. *(Unit 1)*
3. Manipulate Boolean logic using truth tables and mathematical expressions. *(Unit 2 and 3)*
4. Analyze combinational logic circuits using AND, NOT, OR, NOR, NAND and XOR logic gates. *(Unit 2 and 3)*
5. Simplify combinational logic circuits and Boolean algebra. *(Unit 2 and 3)*
6. Simplify logic expressions (in the form of minterms and maxterms) using Karnaugh Maps. *(Unit 4 and 5)*
7. Translate Boolean logic into physical logic circuits. *(Unit 4 and 5)*
8. Use universal NAND and NOR gates to realize logic expressions. *(Unit 7 and 8)*
9. Be able to analyze SR latches. *(Unit 11)*
10. Be able to design and analyze D and JK flip-flops. *(Unit 11)*
11. Use flip-flops (JK, D-type, etc.) in the design of counters and shift registers. *(Unit 12)*
12. Implement logic circuits with multiplexers, demultiplexers, encoders and decoders. *(Unit 9)*

Grading:
90% - 100%	A
80% - 89%	B
70% - 79%	C
60% - 69%	D
0% - 59%	F

The individual components of the class will be weighted as follows:

Homework/Quizzes	20%
Labs	25%
Midterm Exam	15%
Midterm Exam2	15%
Final Exam*	25%

*The Final must be taken to pass the course.

Grades will be displayed on the D2L, assigned to each student by his or her tech ID. It is important that you follow your progress in the course.

Academic Dishonesty: Cheating and Plagiarism will be dealt with in a manner that is consistent with the action. The severity of the penalty may be a simple reprimand, failure for that assignment, or may result in failure of the course. The goal is for you to learn the material. If you are experiencing trouble in the course discuss it with the instructor or teaching assistants. **All work handed in must be your own.**

Homework: Assignments are due at the beginning of class on the day stated. In the event a hardcopy cannot be turned in at that time, an e-mail containing your completed and finished assignment as a word document, jpeg, or pdf will suffice until you can turn in the hardcopy. It should be expected that late assignments will be penalized at a rate of at least 15% per day. A week after the due date the assignments will no longer be accepted.

Exams: The exams will be given at the time to be scheduled. If you cannot make that time, talk to the instructor ahead of time to make alternate arrangements. Unexcused absence will result in zero credit. For extenuating circumstances, a student's final exam percentage will be used in lieu of the missed exam. No electronic devices other than a calculator will be allowed during the exams including (but not limited to): phones, PDAs, MP3/CD players.

ADA: It is the intent of the instructor of this course to provide a learning environment that is as conducive to learning and the expression of abilities as is possible. If any student in this course has any condition that requires special accommodation to allow them to master or demonstrate mastery of concepts they are asked to contact the instructor as soon as possible.