Analog to Digital Conversion - increase comparison voltage in steps
Digital Input to ladder network - switches connect a voltage source to a resistor if the input is a “1” or to ground if the input is a “0”.

- Code = 11 = 3
- 5V/4 = 1.25V per step
- Vo = 3.75

- Code = 10 = 2
- Vo = 2.5

- Code = 01 = 1
- Vo = 1.25
For a reference voltage of 24V,

\[ 2^5 = 32 \]

\[ \frac{24V}{32} = 0.75 \text{ V/step} \]

\[ V_o = 0.75V(0*2^4 + 1*2^3 + 0*2^2 + 1*2^1 + 1*2^0) = 0.75V(0 + 8 + 0 + 2 + 1) = 0.75(11) = 8.25 \]

For a code of 01011 the result is \( 31 * 0.75 = 23.25 \)
Using the 5-bit A/D above to convert 16.9V to digital

\[
16.9/0.75 = 22.53
\]

Round up to 23

\[
\begin{align*}
23/2 &= 11 + 1 & 1*2^0 &= 1 \\
11/2 &= 5 + 1 & 1*2^1 &= 2 \\
5/2 &= 2 + 1 & 1*2^2 &= 4 \\
1/2 &= 0 + 1 & 0*2^3 &= 0 \\
\end{align*}
\]

\[
1*2^4 = 16
\]

23
Capacitor $C$ charges through $R_A + R_B$

Capacitor $C$ discharges through $R_B$

$\frac{2}{3} V_{CC}$

$\frac{1}{3} V_{CC}$

$f \approx \frac{1.44}{(R_A + 2R_B) C}$
Phase Locked Loop

Input signal $V_i / f_i$ → Phase detector $V_e / f_i + f_o$ → Low-pass filter $f_i - f_o$ → Amplifier → Output signal

At VCO center frequency, $f_o$
Linear-Digital ICs

FSK Decoder

![Diagram of an FSK Decoder circuit with a PLL and comparator. The diagram includes components such as resistors (5 kΩ, 600 Ω), capacitors (0.1 μF, 0.05 μF, 0.02 μF, 0.01 μF), and an input frequency selector (1070 Hz or 1270 Hz). The output is marked with the conditions: SPACE = +14 V, MARK = -5 V.]
Input 1A

Strobe S

Input 2A

Output 1Y

Output 2Y

(Y = \overline{A \cdot S})
<table>
<thead>
<tr>
<th></th>
<th>Current Loop</th>
<th>RS-232-C</th>
<th>TTL</th>
</tr>
</thead>
<tbody>
<tr>
<td>MARK</td>
<td>20 mA</td>
<td>-12 V</td>
<td>+5 V</td>
</tr>
<tr>
<td>SPACE</td>
<td>0 mA</td>
<td>+12 V</td>
<td>0 V</td>
</tr>
</tbody>
</table>
(b) RS-232-C to TTL interface
TTY output

Opto-isolator

20-mA current loop to TTL interface

TTY input
The diagram shows a circuit with two transistors, $Q_1$ and $Q_2$, connected in a way that determines the output voltage based on the state of $Q_1$ and $Q_2$.

### Table of Output States

<table>
<thead>
<tr>
<th>$Q_1$</th>
<th>$Q_2$</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Off</td>
<td>Off</td>
<td>Open circuit</td>
</tr>
<tr>
<td>Off</td>
<td>On</td>
<td>0 V</td>
</tr>
<tr>
<td>On</td>
<td>Off</td>
<td>+5 V</td>
</tr>
</tbody>
</table>

The circuit includes a resistor $R$ and a power source of +5 V. The output voltage is determined by the states of $Q_1$ and $Q_2$.